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CHARACTER PATTERN SIGNAL RECEIVING UNIT
[MOJI·ZUKEI SHINGO JUSHIN SOCHI]

Hidekazu Tsuboka, et al.

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INVENTOR	(72):	TSUBOKA; HIDEKAZU, ET AL.
APPLICANT	(71):	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
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Specifications /245*

1. Title of the Invention

Character Pattern Signal Receiving Unit

2. Claim(s)

(1) A character pattern signal receiving unit which reproduces and displays a plurality of character pattern signals transmitted at different speeds via different transmission media by blocking the character pattern information to be transmitted by subjecting them to respectively different signal processings, and then adding control information corresponding to each block; said character pattern signal receiving unit characterized by being provided with a means for selecting one of the aforesaid character pattern signals and fetching this selected signal, or it and a clock accompanying it as a set, a means for using the aforesaid fetched clock to convert the information of each aforesaid block into the signal of the character pattern to be displayed, which signal accompanies the aforesaid control information, a storage means for display use which stores at least one field portion of this converted signal, and a display-driving means for reading out the signal stored in this storage means and displaying it on a display means.

(2) The character pattern signal receiving unit of Claim 1 characterized by the display-driving means being applied to a display means by switching or superposing a signal representing a character pattern read out from the storage means for display use to/on a picture signal of a broadcast television signal.

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*Number in the margin indicates pagination in the foreign text.

(3) The character pattern signal receiving unit of Claim 1 characterized by varying the position displayed on the display means or varying the display method by controlling the position of read-out thereof and the time at which read-out starts while reading out the stored signal from the storage means for display use.

(4) The character pattern signal receiving unit of Claim 1 characterized by the signal-converting means comprising a storage means for converting the speed at which the signal selected by using the selected clock is written, and a means for reading out the aforesaid signal at a different speed than the writing speed of this storage means, converting the information corresponding to the control information to the signal of the character pattern to be displayed, and writing it to the storage means for display use at a speed different from the read-out speed thereof.

(5) The character pattern signal receiving unit of Claim 1 characterized by the storage means for speed conversion use comprising a memory circuit able to independently execute writing and read-out.

3. Detailed Specifications

Owing to diversified information, there has been a movement where more detailed information services are being provided. That is, for television broadcasts, telephones, CATVs, and the like, new information services unavailable in the past are now provided, and bidirectional request services or the like for broadcasting voice, character patterns, still pictures, and the like are being considered.

Under such circumstances, an object of the present invention is to obtain an effective character pattern signal receiving unit, with a household

television set as the terminal, thus enabling reception of character pattern information transmitted from the aforesaid respective media.

The problems to be solved in order to achieve the object as described above are to easily perform (1) a speed conversion for converting the speeds of signals transmitted over a transmission line at various transmission speeds to the speed at which they are displayed on a television set and (2) a conversion of character pattern information, which had been converted to a code appropriate for each transmission line to transmit it via the aforesaid respective transmission media, into a signal in order to display such information on a television set.

Figure 5 schematically shows a signal route in which **100** to **102** are input terminals for signals transmitted via the aforesaid respective transmission media; **103** is a switching circuit for selectively receiving those signals; **104** is a signal processing circuit for converting a transmitted signal to a signal for display on a television set **106**; and **105** is display memory for storing this converted signal and converting it to the speed for display on the television set **106**. Here, the signal processing circuit **104** discriminates if the transmitted signal is a code signal for displaying a character or a character pattern thereof, a luminance signal or color signal or one transmitted after being subjected to band-compression encoding, or if the determination is YES, which band-compression method the signal was subjected to, and so forth, then performs the corresponding decoding, and converts it to a signal for display on the television set **106**. At this time, providing individual processing circuits for performing decoding respectively causes the unit to become extremely complex. Therefore,

simplification of a circuit configuration shall be planned with the use of a microcomputer in the present invention.

Hence, the switching circuit is characterized by selecting one character pattern information service, writing information to a buffer memory according to the clock of the selected information, then reading it from the buffer memory at the processing speed of the central processing unit, performing a corresponding decoding, and transmitting this to display memory.

A practical example of the present invention will now be described in more detail on the basis of the drawings.

Figure 1 is a drawing showing a system for transmitting a character pattern. (a) is system using a telephone and (b) is a system for teletext broadcasting. These transmission systems are called packet systems, which block the information to be transmitted and then transmit the blocks by adding the control information required for each block. In (a), **46** is blocked character pattern data and **45** is control information thereof. In (b), **47** is a horizontal synchronizing signal; **48** is a color burst; **49** is control information; and **50** is blocked character pattern information. The control information **45** and **49** includes information for matching the clock phase for handling information at a terminal, information showing what kind of format the data in the continuously transmitted blocks was encoded in, and so forth. For example, succeeding character information, such as information as to whether it was sent as a character code or the character pattern itself, whether or not band-compression has been performed, or if it is a luminance signal or color signal, is contained in the control

information. Moreover, in teletext broadcasting, a code is also included for channel selection.

On the receiver side, this control information is restored to a video signal based on the following succeeding data. This procedure is performed for each of the aforesaid blocks. In teletext broadcasting, this signal is sent in a vertical blanking period.

Figure 2 is a block diagram showing the principal part of a character pattern signal receiving unit able to select and receive a teletext broadcast and telephone character pattern information directory service ['information' and 'directory' are misspelled in source] transmitted in the above format.

1 in the drawing is a telephone circuit; **2** is a switching switch; **3** is a telephone set; and **4** is a demodulator. This part is used for receiving a telephone character pattern information directory. A request sent from the telephone set **3** by means of pushbuttons or voice is sent to an information center (not shown) through the telephone circuit **1**, and at the information center, the requested character patterns are sent to terminals via the telephone circuit **1**. These character patterns are transmitted in accordance with FS and PS, but the demodulator **4** restores them to the original character pattern information, and at the same time, and reproduces the clock and outputs it to terminals **5** and **6**, respectively.

Meanwhile, in teletext broadcasting, the number of the channels selected and received by a tuner (not shown) and on which teletext broadcasting are performed is transmitted to a terminal **11** via a VIF circuit (not shown), and video signals are obtained through a video detection circuit **12**.

14 is a synchronizing separator circuit, which separates the vertical/horizontal synchronizing signals from the output of the video detection circuit **12**. A sampling gate generating circuit **15** generates a gate signal for pulling out the period when the character broadcast is transmitted after this synchronizing signal. If this gate signal and the signal subjected to waveform generation by a waveform generating circuit **13** from the output of the video detection circuit **12** are set to AND in an AND circuit **16**, only the control information and data of the part where the character broadcast is multiplexed is output to a terminal **17**. Meanwhile, a color synchronizing [misspelled in source] circuit **19** reproduces a color subcarrier, supplies it to a color demodulation circuit **21**, and at the same time, to a clock generation circuit **20**. The clock generation circuit **20** generates a clock for pulling the aforesaid character signal from the color subcarrier signal, and its phase is controlled by a phase-matching signal contained in the aforesaid control information according to the output of the AND circuit **16**. Thereby, in teletext broadcasting, the character pattern data and clock are obtained respectively at the terminals **17** and **18**.

A CPU clock generation circuit **22** is a circuit which generates the clock of a CPU **35** synchronized with vertical/horizontal synchronizing signals. The output thereof is supplied to the CPU **35**.

A data switching circuit **7** switches the telephone character pattern information obtained thereby with the accompanying clock or the clock accompanying the character pattern information by teletext broadcasting.

It is generally convenient to handle the CPU, memory, and the like in 8-bit units, and the serial output from the data switching circuit **7** is converted to 8-bit parallel signals in a serial/parallel conversion shift register **8**. The 8-bit converted signals are input into a FIFO **9**. This is a First-In-First-Out memory where writing and read-out are performed by independent clocks. A 1/8 counter **10** divides the clock chosen by the data switching circuit **7** by eight and provides a write clock to the FIFO **9**. The contents of the FIFO **9** are read out by a clock from a CPU **35**, and the read-out data is fetched by the CPU **35** and converted to character pattern information for display on a television set in accordance with the procedure pre-programmed into a ROM **73** corresponding to the aforesaid control information. Conversion of the transmitted signal speed and the processing speed of the CPU **35** is performed in the FIFO **9**. The resulting signals processed and converted by the above-mentioned CPU **35** are stored separately in a luminance signal memory **25** and a color signal memory **27**, depending if they are a luminous signal or a color signal. Such memory can be constituted to store a plurality of fields by increasing their capacities.

A display counter **24** is a counter which provides a read-out address in the aforesaid memory while reading out the contents in the aforesaid luminance signal memory **25** and color signal memory **27** and displaying them on a CRT **31**. The initial value and cycle of the count synchronized with the output from the clock generation circuit **20** are controlled by the CPU **35**. That is, when they are displayed on the CRT **31**, various display

methods such as displaying the contents in memory **25** and **27** all at once, one line at a time, by scrolling them, and so forth have been considered, but these display methods are chosen arbitrarily by controlling the address method for the display counter **24** in the memory **25** and **27**.

In order to obtain a video signal, a parallel/serial conversion shift register **26** converts the 8-bit parallel output from the luminance signal memory **25** to a serial output. Figure 4(a) shows a case in which a character is displayed on part of a television field. When number 74 part on the field is scanned by an electron beam of a CRT **31**, **76** in Fig. 4(b) denotes an output **41** from the shift register **26**. That is, when the high electric potential and the background are scanned when the character portion is scanned, the output **41** is produced at a low potential. **75** denotes the temporal relationship between the **74** part was pulled out and the output **41** from the shift register **26**.

A display signal generation circuit **28** generates a R (red), a G (green) and a B (blue) primary color signal with respect to the character pattern from the output from the parallel/serial conversion shift register **26**, a color signal memory **27**, and an output control circuit **71**. A detailed configuration thereof is shown in Fig. 3. **61** to **63** and **65** to **67** are AND circuits; **64** is an inverter; and **68** to **70** are OR circuits. The input/output terminal numbers correspond to those shown in Fig. 2. **38** to **40** denote outputs from the color signal memory **27** which determine the colors of the display character pattern, and **55** to **57** denote the output from the output control circuit **71** which determines the background of the display

character pattern, respectively. For example, terminals **58** to **60** correspond to the respective R, G, and B signals. When the output **41** from the parallel/serial conversion shift register **26** is at a high potential, the AND circuits **65** to **67** close so the background color becomes black. At this time, if the output **38** from the color signal memory is high in potential and **39** and **40** are low in potential, corresponding to the color red of the character, a terminal **58** is high in potential and terminals **59** and **60** become low in potential, and the display color becomes red. Since **41** that is high in potential is a situation in which the scanning lines of the CRT **31** just scan the sections of the character pattern with lines, as is seen from the description in Figure 4, the character pattern is colored red at this time. Assuming only terminal **57** out of the terminals **58** to **60** is low in potential, only the **60** out of terminals **58** to **60** is high in potential when the **41** is low in potential, so the display color becomes blue. Since the **41** that is high in potential is a situation in which the scanning lines of the CRT **31** scans the background sections of the character pattern outside the sections with lines, the background color at this time becomes blue. The color of the character pattern can be determined by the outputs **38** to **40** from the color signal memory **27** and the color of the background can be determined by the outputs **55** to **57** from the data switching circuit **7**, which colors can be not only R, G and B, but also cyan, magenta, yellow, or the like by combinations thereof.

A display signal switching circuit **29** is a circuit which switches or superposes a television signal demodulated by the color demodulation

circuit **21** to/on the aforesaid character pattern display signal. By switching these signals, a conventional television broadcast may be switched to or superposed on a character pattern information service broadcasted or sent over a telephone circuit, and displayed on the CRT **31**.

A gate circuit **23** generates a signal for resetting the shift register **26** for ascertaining the display position of the character pattern with respect to the horizontal/vertical synchronizing signal.

A viewer operates a keyboard **37** when switching between any television broadcast, telephone character pattern information service and teletext broadcast, when selecting a program in a teletext broadcast, when selecting a display method, such as a full-field display or scrolling display, when indicating a background color, when desiring to stop refreshing a field, when erasing a field, and so forth. The viewer also transmits the input from this keyboard **37**, which is common for a telephone character pattern information service and teletext broadcast to the CPU **35** via an input control circuit **36**, and controls the data switching circuit **7**, display counter **24**, display signal generation circuit **28**, and display signal switching circuit **29**, respectively, as mentioned above, via output control circuits **32**, **33**, **71**, and **31**.

ROM **73** stores the programs to be executed by the CPU **35** and RAM **72** is used for temporarily storing information required while executing the aforesaid programs.

According to the present invention as also seen from the practical example described above, an inexpensive television set can be realized

because it has, for the most part, common circuits able to receive both the aforesaid telephone character pattern information service and teletext broadcast at different transmission speeds and signal modes.

4. Brief Explanation of the Drawings

Figure 1 is a waveform chart for explaining a transmission system for a character pattern information service and teletext broadcast with a telephone; Figure 2 is a block diagram of the principal part showing a practical example of the present invention; Figure 3 is a circuit configuration diagram showing the principal part in Fig. 2; Figure 4 is a drawing showing a waveform corresponding to a character pattern on a field; and Figure 5 is a block diagram for describing a summary of the present invention.

1: telephone circuit; 2: changeover switch; 3: telephone set; 4: demodulator; 7: data switching circuit; 8: serial/parallel conversation shift register; 9: FIFO; 10: 1/8 counter; 12: video detection circuit; 13: waveform generation circuit; 14: synchronous separating circuit; 15: sampling gate generating circuit; 16: AND circuit; 19: color synchronization circuit; 20: clock generation circuit; 21: color demodulation circuit; 22: CPU clock generation circuit; 23: gate circuit; 24: display counter; 25: luminance signal memory; 26: parallel/serial conversion shift register; 27: color signal memory; 28: display signal generation circuit; 29: display signal switching circuit; 30, 32, 33: output control circuits; 31: CRT; 35: CPU; 36: input control circuit; 37: keyboard; 72: RAM; 73: ROM

Figure 1

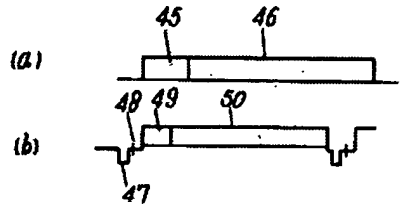

Figure 2

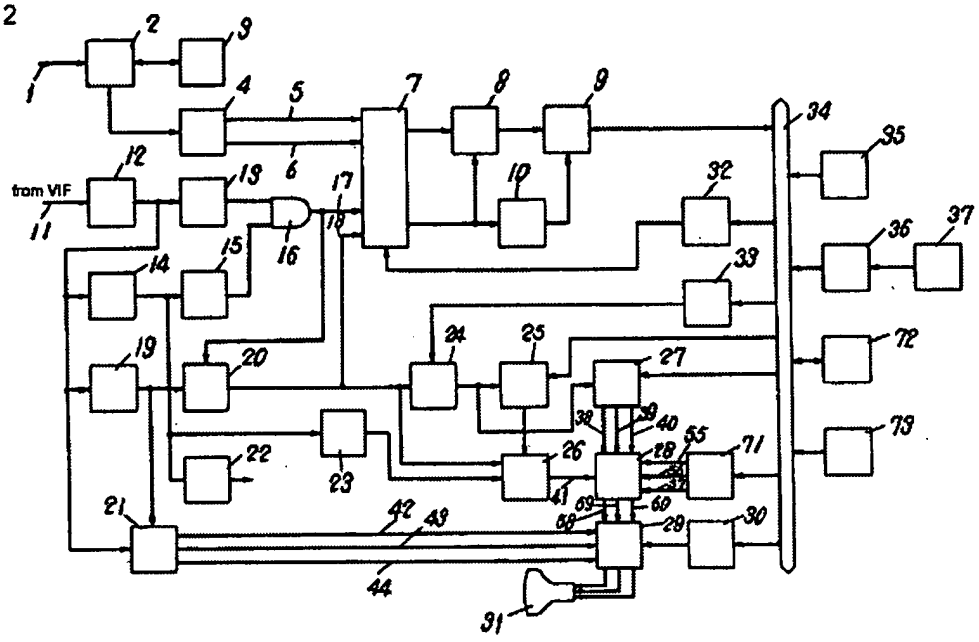

Figure 3

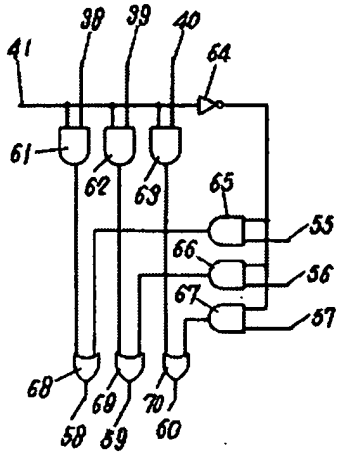

Figure 4

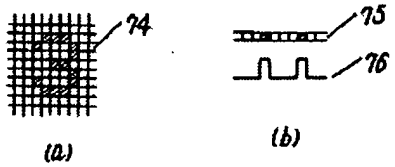

Figure 5